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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,602	JEDDELOH, JOSEPH	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated November 16, 2004.

2. Claims 1-53 are presented for examination.

3. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 1-2, 6, 13-15, 18-25, 31, 35, 43-44, and 48

5. Claims 1-2, 6, 13-15, 18-25, 31, 35, 43-45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., U.S. Patent 6226729, hereinafter Stevens, in view of, Olarig et al., U.S. Patent 6134638, hereinafter Olarig.

6. Stevens discloses a method of selecting an operating speed [channel frequency] of a memory module interface [interfaces 530, 540, 544] in a computer system [fig.5], said system comprising a central processing unit [processor 595], a memory controller [MCH 500], and at least one memory module [RIMM 570] comprising a serial presence detect memory [572], said method comprising:

- Counting the number of said memory modules [fig.8a, 850; col.12, ll.62-67; table 4].

- Generating a clock frequency to provide an operating speed of said memory module interface [col.13, ll.41-49].
- Selecting one of said operating speeds of said memory module interface in accordance with said counting [col.13, ll.41-45].

7. Stevens did not disclose explicitly generating multiple clock frequencies.

8. Olarig discloses a method of selecting an operating speed of a memory module interface in a computer system [100], said system comprising a central processing unit [processor 102], a memory controller [200], and at least one memory module [SDRAM 114], said method comprising:

- Generating multiple clock frequencies [503, 505, 507, 509] to provide selectable operating speeds [memory clock] of said memory module interface [fig.6; col.11, l.39 – col.12, l.38].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens to include generating multiple clock frequencies as taught by Olarig, in order to obtain the system capable of generating multiple clock frequencies to provide selectable operating speeds of the memory module interface. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to operate memory devices with different operating speeds [Olarig: col.2, ll.60-67].

10. As to claim 2, Stevens and Olarig disclose said selecting comprises generating memory module interface signals comprising clock, address, and data signals at a frequency based on said

memory module count [Stevens: col.11, l.35 – col.12, l.22; col.13, ll.41-56; Olarig: col.2, ll.20-34].

11. As to claim 6, Olarig discloses said characteristic comprises a manufacturer of said memory module [table 1; col.10, ll.25-37].

12. In re claim 13, Stevens discloses a computer system [fig.5] comprising:

- A central processing unit [processor 595].
- A memory controller [MCH 500] including a memory module interface [interfaces 530, 540, 544].
- At least one memory module [RIMM 570] including a serial presence detect memory [572].
- Wherein said memory controller:
    - Accesses said serial presence detect memory [col.11, l.66 – col.12, l.14].
    - Keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory [fig.8a, 850; col.12, ll.62-67; table 4].
    - Selects one of the clock frequencies for driving said memory module interface based on at least a final tally of the number of said memory modules [col.13, ll.41-45].

13. Stevens did not disclose explicitly generating multiple clock frequencies.

14. Olarig discloses a computer system [100] comprising:

- A central processing unit [processor 102].
- A memory controller [200].

- At least one memory module [SDRAM 114].
- Wherein said memory controller:
    - Generates multiple clock frequencies [503, 505, 507, 509] [fig.6; col.11, l.39 – col.12, l.38].

15. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens to include generating multiple clock frequencies as taught by Olarig, in order to obtain the system capable of generating multiple clock frequencies to provide selectable operating speeds of the memory module interface. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to operate memory devices with different operating speeds [Olarig: col.2, ll.60-67].

16. As to claim 14, Stevens discloses that the central processing unit is a microprocessor [processor 595].

17. As to claim 15, Stevens discloses the memory controller that obtains information from said serial presence detect memory that includes at least one characteristic of each said memory module [col.11, l.66 – col.12, l.14].

18. As to claim 18, Olarig discloses said characteristic comprises a manufacturer of said memory module [table 1; col.10, ll.25-37].

19. In re claim 25, Stevens discloses a computer system [fig.5] comprising:

- A central processing unit [processor 595].
- At least one memory module [RIMM 570] including a serial presence detect memory [572].

- Memory controller means [MCH 500] including memory module interface means [interfaces 530, 540, 544].
- Wherein said memory controller means:
    - Accesses said serial presence detect memory [col.11, l.66 – col.12, l.14].
    - Keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory [fig.8a, 850; col.12, ll.62-67; table 4].
    - Selects one of the clock frequencies for driving said memory module interface based on at least a final tally of the number of said memory modules [col.13, ll.41-45].

20. Stevens did not disclose explicitly generating multiple clock frequencies.

21. Olarig discloses a computer system [100] comprising:

- A central processing unit [processor 102].
- Memory controller means [200].
- At least one memory module [SDRAM 114].
- Wherein said memory controller means:
    - Generates multiple clock frequencies [503, 505, 507, 509] [fig.6; col.11, l.39 – col.12, l.38].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens to include generating multiple clock frequencies as taught by Olarig, in order to obtain the system capable of generating multiple clock frequencies to provide selectable

operating speeds of the memory module interface. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to operate memory devices with different operating speeds [Olarig: col.2, ll.60-67].

23. In re claim 31, Stevens discloses a memory controller [MCH 500] comprising a memory module interface [interfaces 530, 540, 544] to at least one memory module [RIMM 570], said memory module [RIMM 570] including a serial presence detect memory [572], wherein said memory controller:

- Accesses said serial presence detect memory [col.11, l.66 – col.12, l.14].
- Keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory [fig.8a, 850; col.12, ll.62-67; table 4].
- Provides a memory module at a clock rate based on at least a final tally of the number of said memory modules [col.13, ll.41-45].

24. Stevens did not disclose explicitly generating multiple clock frequencies.

25. Olarig discloses a memory controller [200] that:

- Generates multiple clock frequencies [503, 505, 507, 509] [fig.6; col.11, l.39 – col.12, l.38].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens to include generating multiple clock frequencies as taught by Olarig, in order to obtain the system capable of generating multiple clock frequencies to provides a memory module at a clock rate based on at least a final tally of the number of said memory modules. One of

ordinary skill in the art would have been motivated to make such a combination as it provides a way to operate memory devices with different operating speeds [Olarig: col.2, ll.60-67].

27. As to claim 35, Olarig discloses said characteristic comprises a manufacturer of said memory module [table 1; col.10, ll.25-37].

28. In re claims 43-44 and 48, Stevens and Olarig discloses the method as discussed above in reference to claims 1-2 and 6. Therefore, Johnson, Stevens and Olarig disclose the apparatus to which the method is operated on.

Re Claim 3-5, 7-12, 16-17, 19-20, 26-30, 32-34, 36-39, 41, 45-47, 49-50, 51-53

29. Claims 3-5, 7-12, 16-17, 19-20, 26-30, 32-34, 36-39, 41, 45-47, 49-50, 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Olarig as applied to claim 1 above, and further in view of Johnson et al., U.S. Patent 5577236, hereinafter Johnson.

30. In re claim 3, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 1. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

31. Johnson discloses a method comprising:

- Obtaining information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors 2-4] of a memory module, wherein a selecting comprises selecting one of the clocks in accordance with one of said counting [factor 1] and said characteristic [col.8, ll.33-45; col.9, ll.4-18].

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the

system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module, wherein a selecting comprises selecting one of the operating speeds in accordance with one of said counting and said characteristic. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

33. As to claim 4, Johnson discloses said characteristic comprises the number of components [memory circuits] in each said memory module [col.9, ll.9-10].

34. As to claim 5, Johnson discloses said characteristic comprises a speed grade [sort] of said memory module [col.9, ll.17-18].

35. As to claim 7, Johnson discloses said characteristic comprises a type of said memory module [col.8, ll.33-41].

36. As to claim 8, Johnson discloses said characteristic comprises a physical layout of signal connections between said memory controller and said memory module [col.9, ll.11-16].

37. In re claim 9, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 1. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

38. Johnson discloses a method comprising:

- Obtaining information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors 2-4] of a memory module [col.8, ll.33-45; col.9, ll.4-18].

- Selecting the clock of the memory module interface in accordance with at least one of said counting [factor 1] and said obtaining information [col.9, ll.4-18].

39. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module and selecting the operating speed of the memory module interface in accordance with at least one of said counting and said obtaining information. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

40. As to claim 10, Johnson discloses said characteristic comprises a type of said memory module [col.8, ll.33-41].

41. In re claim 11, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 1. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

42. Johnson discloses a method comprising:

- Obtaining information from a serial presence detect memory [flash memory] that includes at least the number of components [memory circuits] in each memory module [col.8, ll.33-45; col.9, ll.4-18].
- Selecting the clock of the memory module interface in accordance with said obtaining information [col.9, ll.4-18].

43. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least the number of components in each memory module and selecting the operating speed of the memory module interface in accordance with said obtaining information. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

44. In re claim 12, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 1. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

45. Johnson discloses a method comprising:

- Obtaining information from a serial presence detect memory [flash memory] that includes at least a speed grade [sort] of a memory module [col.8, ll.33-45; col.9, ll.4-18].
- Selecting the clock of the memory module interface in accordance with said obtaining information [col.9, ll.4-18].

46. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least a speed grade of a memory module and selecting the operating speed of the memory

module interface in accordance with said obtaining information. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

47. In re claims 16-17 and 19-20, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 1. Stevens and Olarig did not discuss the details of the characteristics of the memory module.

48. Johnson discloses a system [fig.3] comprising:

- As to claim 16, the characteristic that comprises the number of components [memory circuits] in each said memory module [col.9, ll.9-10].
- As to claim 17, the characteristic that comprises a speed grade [sort] of said memory module [col.9, ll.17-18].
- As to claim 19, the characteristic that comprises a type of said memory module [col.8, ll.33-41].
- As to claim 20, the characteristic that comprises a physical layout of signal connections between said memory controller and said memory module [col.9, ll.11-16].

49. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes the various characteristics of the memory module. One of ordinary skill in the art would have been

motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

50. In re claim 26, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 25. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

51. Johnson discloses a memory controller [302] that:

- Obtains information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors 2-4] of a memory module [col.8, ll.33-45; col.9, ll.4-18].
- Provides a memory module interface means with a clock based on at least a final tally of the number of said memory modules and said obtained information [col.8, ll.33-45; col.9, ll.4-18].

52. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module to provide a memory module interface means with a clock based on at least a final tally of the number of said memory modules and said obtained information. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

53. As to claim 27, Johnson discloses said characteristic comprises a type of said memory module [col.8, ll.33-41].

54. As to claim 28, Johnson discloses said characteristic comprises a physical layout of signal connections between said memory controller and said memory module [col.9, ll.11-16].

55. In re claim 29, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 25. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

56. Johnson discloses a memory controller [302] that:

- Obtains information from a serial presence detect memory [flash memory] that includes at least the number of components [memory circuits] in each memory module [col.8, ll.33-45; col.9, ll.4-18].
- Provides a memory module interface means with a clock based on at least a final tally of the number of said memory modules and said obtained information [col.8, ll.33-45; col.9, ll.4-18].

57. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least the number of components in each memory module and providing a memory module interface means with a clock based on at least a final tally of the number of said memory modules and said obtained information. One of ordinary skill in the art would have been

motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

58. In re claim 30, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 25. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

59. Johnson discloses a memory controller [302] that:

- Obtains information from a serial presence detect memory [flash memory] that includes at least a speed grade [sort] of said memory module [col.9, ll.17-18].
- Provides a memory module interface means with a clock based on at least a final tally of the number of said memory modules and said obtained information [col.8, ll.33-45; col.9, ll.4-18].

60. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least the number of components in each memory module and providing a memory module interface means with a clock based on at least a final tally of the number of said memory modules and said obtained information. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

61. In re claim 32, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 31Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

62. Johnson discloses a memory controller [302] that:

- Obtains information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors 2-4] of a memory module, wherein the clock is also based on said characteristic [col.8, ll.33-45; col.9, ll.4-18].

63. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module, wherein a selecting comprises selecting one of the operating speeds in accordance with one of said counting and said characteristic. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

64. As to claim 33, Johnson discloses said characteristic comprises the number of components [memory circuits] in each said memory module [col.9, ll.9-10].

65. As to claim 34, Johnson discloses said characteristic comprises a speed grade [sort] of said memory module [col.9, ll.17-18].

66. As to claim 36, Johnson discloses said characteristic comprises a type of said memory module [col.8, ll.33-41].

67. As to claim 37, Johnson discloses said characteristic comprises a physical layout of signal connections between said memory controller and said memory module [col.9, ll.11-16].

68. In re claim 38, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 25. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

69. Johnson discloses a memory controller [302] that:

- Obtains information from a serial presence detect memory [flash memory] that includes at least one characteristic [factors 2-4] of a memory module [col.8, ll.33-45; col.9, ll.4-18].
- Selects one of the clocks for driving a memory module interface based on at least one of a final tally of the number of said memory modules and said obtained information [col.8, ll.33-45; col.9, ll.4-18].

70. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module, wherein a selecting comprises selecting one of the operating speeds in accordance with at least one of said counting and said characteristic. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

71. As to claim 39, Johnson discloses said characteristic comprises a speed grade [sort] of said memory module [col.9, ll.17-18].

72. In re claim 41, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 25. Stevens and Olarig did not discuss the details of selecting one of the operating speeds.

73. Johnson discloses a memory controller [302] that:

- Obtains information from a serial presence detect memory [flash memory] [col.8, ll.33-45; col.9, ll.4-18].
- Selects one of the clocks for driving a memory module interface based on said obtained information [col.8, ll.33-45; col.9, ll.4-18].

74. It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes at least one characteristic of a memory module, wherein a selecting comprises selecting one of the operating speeds in accordance with at least one of said counting and said characteristic. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

75. In re claims 45-47 and 49-50, Johnson, Stevens and Olarig disclose the method as discussed above in reference to claims 3-5 and 7-8. Therefore, Johnson, Stevens and Olarig disclose the apparatus to which the method is operated on.

76. In re claims 51-53, Johnson, Stevens and Olarig disclose the method as discussed above in reference to claims 9, 11-12. Therefore, Johnson, Stevens and Olarig disclose the apparatus to which the method is operated on.

Re Claim 21 and 40

77. Claims 21 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Olarig as applied to claims 15 and 31 above, and further in view of Hartwell, U.S. Patent 6724850.

78. In re claim 21, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 15. Stevens and Olarig did not discuss the details of generating different frequencies.

79. Hartwell discloses a computer system [data processing system 100] comprising:

- At least two phase locked loops [PLL 1 and 3] to generate respective clock signals of different frequencies [slow and fast] [col.2, l.52 – col.3, l.10].

80. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens, Olarig, and Hartwell before him at the time the invention was made, to use the phase locked loops taught by Hartwell for the system disclosed by Stevens and Olarig as the phase locked loop taught by Hartwell is a well known circuit suitable for generating different frequencies for the system of Stevens and Olarig. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to generate different frequencies in a system that require different clock speeds [Hartwell: col.1, l.56 – col.2, l.49].

81. In re claim 40, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claim 31. Stevens and Olarig did not discuss the details of generating different frequencies.

82. Hartwell discloses a computer system [data processing system 100] comprising:

- At least two phase locked loops [PLL 1 and 3] to generate respective clock signals of different frequencies [slow and fast] [col.2, l.52 – col.3, l.10].

83. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens, Olarig, and Hartwell before him at the time the invention was made, to use the phase locked loops taught by Hartwell for the system disclosed by Stevens and Olarig as the phase locked loop taught by Hartwell is a well known circuit suitable for generating different frequencies for the system of Stevens and Olarig. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to generate different frequencies in a system that require different clock speeds [Hartwell: col.1, l.56 – col.2, l.49].

Re Claim 22-24, 42

84. Claims 22-24 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartwell, Stevens and Olarig as applied to claims 21 and 41 above, and further in view of Johnson et al., U.S. Patent 5577236, hereinafter Johnson.

85. In re claims 22-24, 42 Hartwell, Stevens and Olarig disclose each and every limitation of the claim as discussed above in reference to claims 21 and 41. Hartwell, Stevens and Olarig did not discuss the details of the characteristics of the memory module.

86. Johnson discloses a system [fig.3] comprising:

- As to claims 22-23, the characteristic that comprises the number of components [memory circuits] in each said memory module [col.9, ll.9-10].
- As to claim 24 and 42, the characteristic that comprises a speed grade [sort] of said memory module [col.9, ll.17-18].

87. It would have been obvious to one of ordinary skill in the art, having the teachings of Hartwell, Johnson, Stevens and Olarig before him at the time the invention was made, to modify the system taught by Hartwell, Stevens and Olarig to include teachings of Johnson, in order to obtain the system capable of obtaining information from a serial presence detect memory that includes the various characteristics of the memory module. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to accurately read data from a memory that may vary in numbers and other attributes [Johnson: col.2, l.46 – col.3, l.50].

Response to Arguments

88. All rejections of claim limitations as filed prior to Amendment dated November 16, 2004 not argued in entirety or substantively in response filed as said Amendment have been conceded by Applicant and the rejections are maintained from henceforth.

89. Applicant's arguments, with respect to claims 1, 13, 25, 31, and 43 have been fully considered but they are not persuasive.

90. Applicant alleges that "neither Stevens nor Olarig discloses or suggests 'selecting one of the operating speeds of said memory module interface'". Firstly, in response to Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231

USPQ 375 (Fed. Cir. 1986). In the instant case, the rejections were based on a combination of Stevens and Olarig to teach each and every limitation. Secondly, in response to Applicant's point that Stevens "does not disclose or suggest generating multiple clocks at different frequencies to provide the selectable operating speeds", Examiner appreciatively points to Applicant's own concession that "Stevens is directed to a method for configuring or initializing a memory device... the frequency of the clock is generated by '***determining*** a channel frequency at which all [memory modules] may operate'" [page 3 of Remarks]. Applicant's own concession of this important point indicates that Stevens does *suggest* the capability to generate multiple different speeds in order to ***determine*** an appropriate speed. The explicit teaching of generating multiple clock frequencies is provided by Olarig.

91. Applicant alleges that "neither Stevens nor Olarig discloses or suggests selecting the operating speed in accordance with the ***counting of the number of memory modules***." Applicant then supports the allegation by asserting that Stevens and Olarig "disclose the generation of one or more clock speeds based on the speed of the memory modules, but not on the ***number of memory modules***". Applicant committed a reasoning error by changing the subject entity [i.e., switching from counting of the number to just the number itself]. Examiner kindly reminds Applicant that there is a significant difference between selecting one of the operating speeds in accordance with the ***act*** of counting of the number of memory modules and selecting one of the operating speeds in accordance with just the number of memory modules. The act of counting as disclosed by Stevens includes querying the memory modules for various device information to assist in the selection of an operating speed – without the act of counting, an operating speed cannot be selected in accordance.

92. Applicant alleges that "neither Stevens nor Olarig provides a motivation for being combined with the other." Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation was asserted as "a way to operate memory devices with different operating speeds" [Olarig: col.2, ll.60-67].

93. Applicant's arguments, with respect to claims 9, 11, 12, 26, 29, 30, 38, 41, 51-53, 21, 40, 23, 24, and 42 have been fully considered but they are not persuasive. In general, Applicant's arguments are direct against the references individually as discussed above. Again, Examiner kindly reminds Applicant that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references

94. All other claims were not argued separately.

95. As demonstrated above, Applicant's arguments are not persuasive and the rejections of all claims are thus maintained.

Conclusion

96. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Tse Chen
February 26, 2005